MF616
3-Phase Brushless DC Motor Controller
Data Sheet

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Revision History:

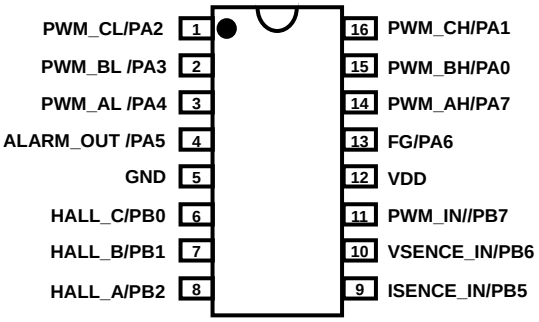
Revision	Date	Description
0.03	2021/01/15	Add pin description
0.04	2021/06/03	Add SOP16 package
0.05	2023/08/03	1. Updated “IMPORTANT NOTICE” 2. Updated DC/AC Characteristics: f_{SYS}, I_{OP}, V_{BRD}, V_{BG}, f_{IHRC}, V_{ADC}, ADclk 3. Updated Chapter 4 (three-phase schematic) 4. Updated PCB layout guideline(Chapter 6)

1. Key Features

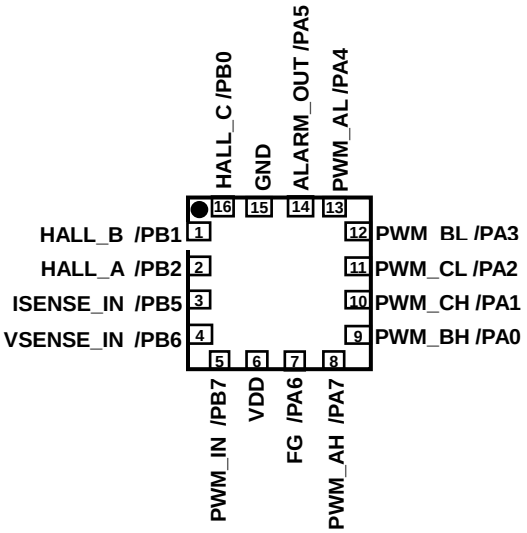
- 3-Phase brushless DC motor with hall IC interface
- PWM or voltage control input
- FG/RD/ALM/RALN/RXX/RRXX output
- Alarm output
- Reverse brake control
- Software hall degree forward and backward
- Close loop or/and open loop control
- Current limit and over-current protection
- Under voltage lock out protection
- Over voltage lock out protection
- Soft-start, lock-protect and auto-restart
- System protection
  - Low-voltage detection with reset
  - Illegal opcode detection with reset
- MTP Programming
  - Support 6-wire factory programming mode
  - Support 4-wire in-system programming mode
- DC Fan Applications
  - Operating voltage range: 3.5V~6V
  - Operating temperature range: -40°C~105°C
- Package Information
  - MF616-Y16: SSOP16 (150mil)
  - MF616-S16: SOP16 (150mil)
  - MF616-1J16A (QFN3*3-16P-0.5pitch)

MF616 is a 3-phase BLDC motor controller based on 8-bit 8-FPPA MCU which can be programmed by 6-wire factory mode or 4-wire ISP mode. MF616 receives motor position signal from Hall IC and can control the six step square wave flexibly to make the best efficiency of the motor. Through the PADAUK patented AP development system, it can easily set any speed curve, output signal and protection parameters etc., and it can observe the motor response online immediately. Using the MF616's development system, it's much easier and adjustable for application.

2. Pin Diagram and Pin Description



MF616-Y16 (SSOP16-150mil)
MF616-S16 (SOP16-150mil)



MF616-1J16A (QFN3*3-16P-0.5pitch)

Pin Name	I/O	Description
PWM_CL / PA2	Output	C output signal to control the low side of motor driver
PWM_BL / PA3	Output	B output signal to control the low side of motor driver
PWM_AL / PA4	Output	A output signal to control the low side of motor driver
ALARM_OUT / PA5	Output	Digital output to motor alarm
GND	-	Ground
HALL_C / PB0	Input	Digital input to sense motor position C
HALL_B / PB1	Input	Digital input to sense motor position B
HALL_A / PB2	Input	Digital input to sense motor position A
ISENSE_IN / PB5	Input	Analog input to sense motor current
VSENSE_IN / PB6	Input	Analog input to sense motor voltage
PWM_IN / PB7	Input	PWM control input
VDD	-	Positive power
FG / PA6	Output	Rotation speed detection
PWM_AH / PA7	Output	A output signal to control the high side of motor driver
PWM_BH / PA0	Output	B output signal to control the high side of motor driver
PWM_CH / PA1	Output	C output signal to control the high side of motor driver

3. Device Characteristics

3.1. Absolute Maximum Ratings

Name	Min	Typ.	Max	Unit	Notes
Supply Voltage (VDD)	3.5		6	V	**Exceed the maximum rating may cause permanent damaged !!**
Input Voltage	-0.3		V_{DD} + 0.2	V	
Operating Temperature	-40		105	°C	
Storage Temperature	-50		125	°C	
Junction Temperature		150		°C	

3.2. DC/AC Characteristics

Symbol	Description	Min	Typ	Max	Unit	Conditions (Ta=25℃)
V_{DD}	Operating Voltage	3.5 4.75	5.0 5.0	6 6	V	-40 °C <Ta<85 °C -40 °C <Ta<105 °C
V_{FSV}	Forbidden V_{DD} startup voltage range	0.7		1.6	V	
V_{PDRV}	V_{DD} power down release voltage			0.7	V	
T_{POR}	V_{DD} power on time (V_{DD} from 0V to 5V)			50	ms	
T_{FSV}	V_{DD} power on time during V_{FSV} range			10	ms	
f_{SYS}	System clock IHRC/2	 0		 8M	Hz	 V_{DD} = 3.3V
I_{OP}	Operating Current		3.5		mA	f_{SYS}=8MIPS@5.0V
I_{PD}	Power Down Current (by ***stopsys*** command)		3 1		uA uA	V_{DD}=5.0V V_{DD}=3.3V
I_{PS}	Power Save Current (by ***stopexe*** command)		0.4		mA	VDD=5.0V; Band-gap, LVD, IHRC, ILRC, Timer16 modules are ON.
V_{IL}	Input low voltage for IO lines	0		0.2V_{DD}	V	
V_{IH}	Input high voltage for IO lines	0.8 V_{DD}		V_{DD}	V	
I_{OL}	IO lines sink current	11	14	17	mA	V_{DD}=5.0V, V_{OL}=0.5V
I_{OH}	IO lines drive current	-8	-10	-12	mA	V_{DD}=5.0V, V_{OH}=4.5V
R_{PH}	Pull-high Resistance		90 170		KΩ	V_{DD}=5.0V V_{DD}=3.3V
V_{BRD}	Low Voltage Detect Voltage * (Brown-out voltage)	3.0	3.3	3.5	V	
V_{BG}	Bandgap Reference Voltage (before calibration)	1.12	1.20	1.28	V	V_{DD}=5V, 25°C
	Bandgap Reference Voltage * (after calibration)	1.17*	1.20*	1.23*		V_{DD}=3.3V ~ 5.5V, -40°C <Ta<105°C*

Symbol	Description	Min	Typ	Max	Unit	Conditions (Ta=25℃)
f_{IHRC}	Frequency of IHRC after calibration *	15.52*	16*	16.48*	MHz	25ºC, V_{DD}=3.3V~5.5V
		14*	16*	17.28*		V_{DD}=3.3V~5.5V, -40ºC <Ta<105ºC*
f_{ILRC}	Frequency of ILRC *	31.5*	33.8*	35*	KHz	V_{DD}=5.0V, Ta=25ºC
		29*	33.8*	38.4*		V_{DD}=5.0V, -40ºC <Ta<85ºC*
		32*	34*	35.5*		V_{DD}=3.3V, Ta=25ºC
		29*	34*	40*		V_{DD}=3.3V, -40ºC <Ta<85ºC*
V_{ADC}	Workable ADC operating Voltage	3.3		6.0	V	
V_{AD}	AD Input Voltage	0		V_{DD}	V	
ADrs	ADC resolution			11	bit	
ADclk	ADC clock period		2		us	3.3V ~ 5.5V
t_{ADCONV}	ADC conversion time (T_{ADCLK} is the period of the selected AD conversion clock)		14		T_{ADCLK}	
AD DNL	ADC Differential NonLinearity		±3*		LSB	
AD INL	ADC Integral NonLinearity		±3*		LSB	
ADos	ADC offset*		3 4		LSB	-40ºC <Ta<85ºC* -40ºC <Ta<105ºC*
t_{INT}	Interrupt pulse width	30			ns	V_{DD} = 5.0V
V_{DR}	RAM data retention voltage*	1.5			V	In power-down mode.
t_{WDT}	Watchdog timeout period (T_{ILRC} is the clock period of ILRC)		4096			misc[1:0]=01
			16384			misc[1:0]=10
t_{SBP}	System boot-up period from power-on		1024		T_{ILRC}	Where T_{ILRC} is the clock period of ILRC
θ_{ja}	Thermal resistance from junction to ambient		75		°C/W	
θ_{jc}	Thermal resistance junction to top of case		25		°C/W	

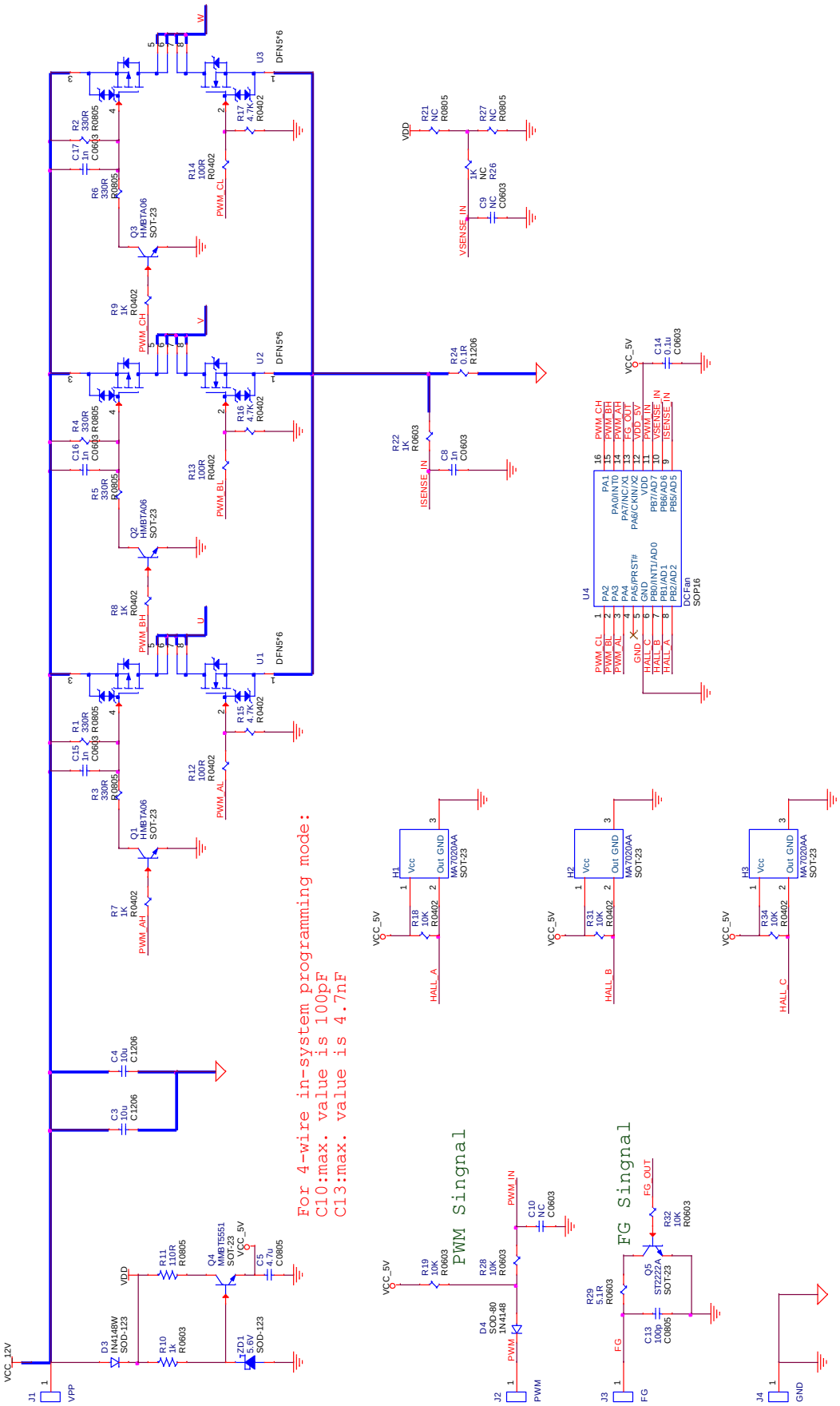
Symbol	Description	Min	Typ	Max	Unit	Conditions (Ta=25℃)
t_{WUP}	System wake-up period					
	Fast wake-up by IO toggle from STOPEXE suspend		128		T_{SYS}	Where T_{SYS} is the time period of system clock
	Fast wake-up by IO toggle from STOPSYS suspend, IHRC is the system clock		128 T_{SYS} + T_{SIHRC}			Where T_{SIHRC} is the stable time of IHRC from power-on.
	Fast wake-up by IO toggle from STOPSYS suspend, ILRC is the system clock		128 T_{SYS} + T_{SILRC}			Where T_{SILRC} is the stable time of ILRC from power-on.
	Normal wake-up from STOPEXE or STOPSYS suspend		1024		T_{ILRC}	Where T_{ILRC} is the clock period of ILRC
HCPos	Comparator offset*	-	±10	±20	mV	
HCPcm	Comparator input common mode*	0		V_{DD}-1.5	V	
HCPspt	Comparator response time**		100	500	ns	Both Rising and Falling
HCPmc	Stable time to change comparator mode		2.5	7.5	us	

*These parameters are for design reference, not tested for every chip.

** Response time is measured with comparator input at (V_{DD}-1.5)/2 -100mV, and (V_{DD}-1.5)/2+100mV

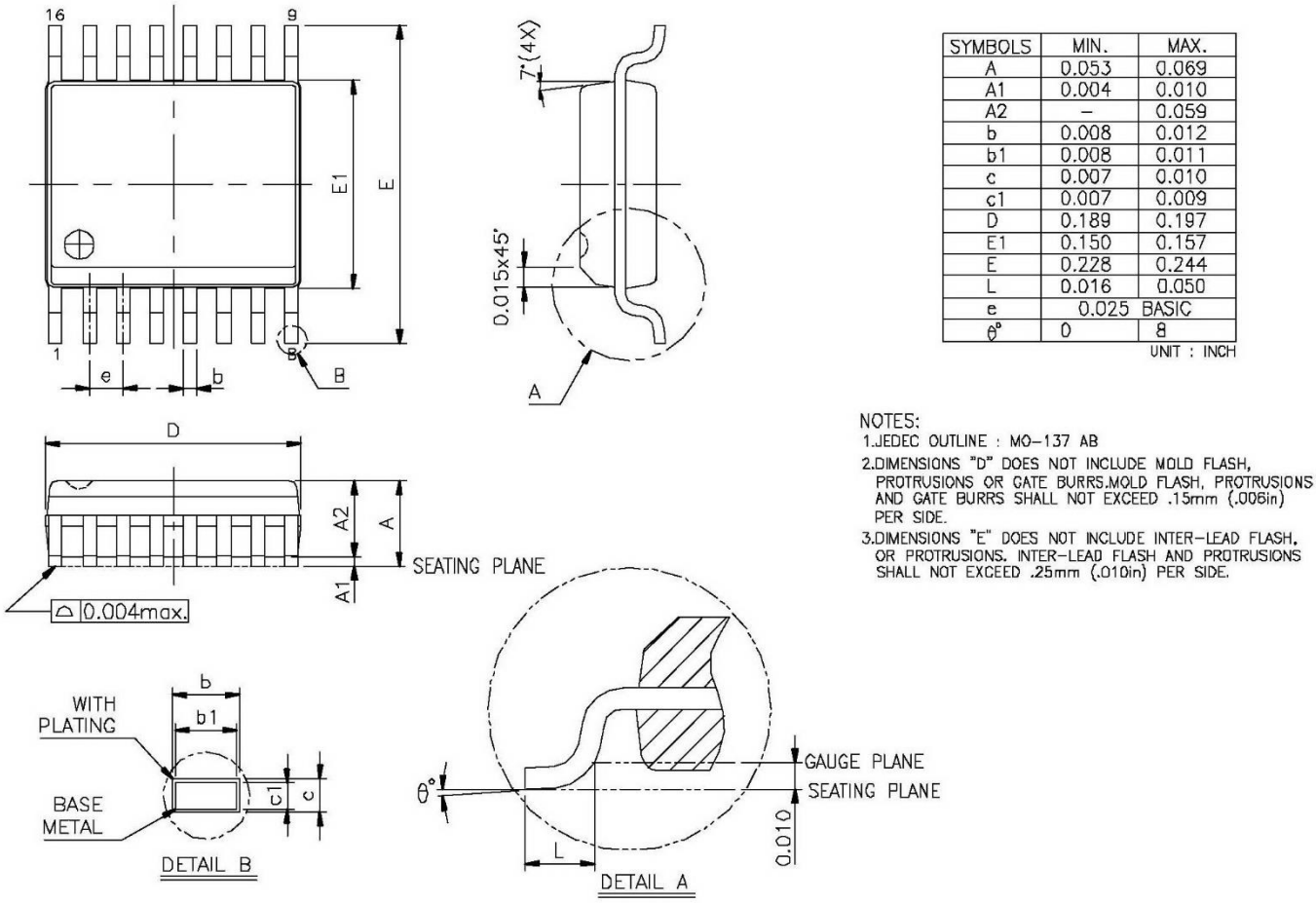
The characteristic diagrams are the actual measured values. Considering the influence of production drift and other factors, the data in the table are within the safety range of the actual measured values.

4. Reference Application Circuit



5. Package Information

5.1. SSOP16 (150mil)

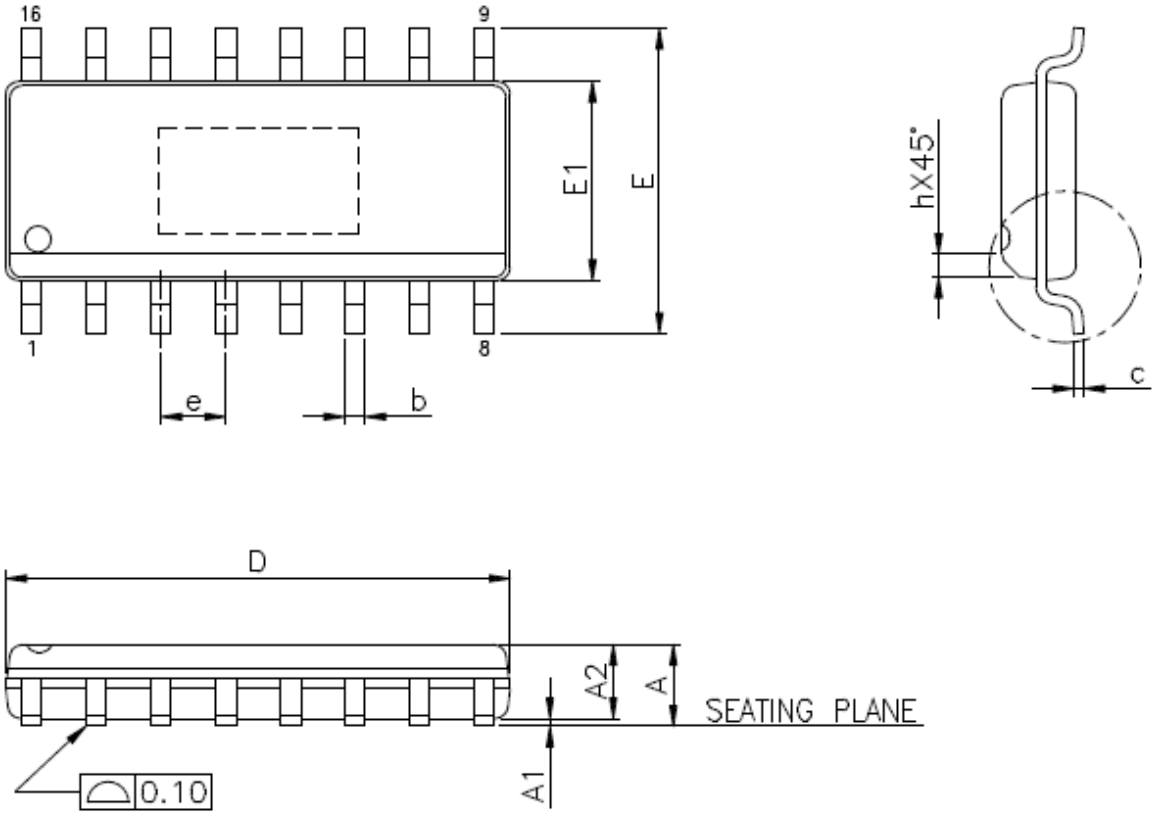


SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
A2	–	0.059
b	0.008	0.012
b1	0.008	0.011
c	0.007	0.010
c1	0.007	0.009
D	0.189	0.197
E1	0.150	0.157
E	0.228	0.244
L	0.016	0.050
e	0.025 BASIC	
θ°	0	8

UNIT : INCH

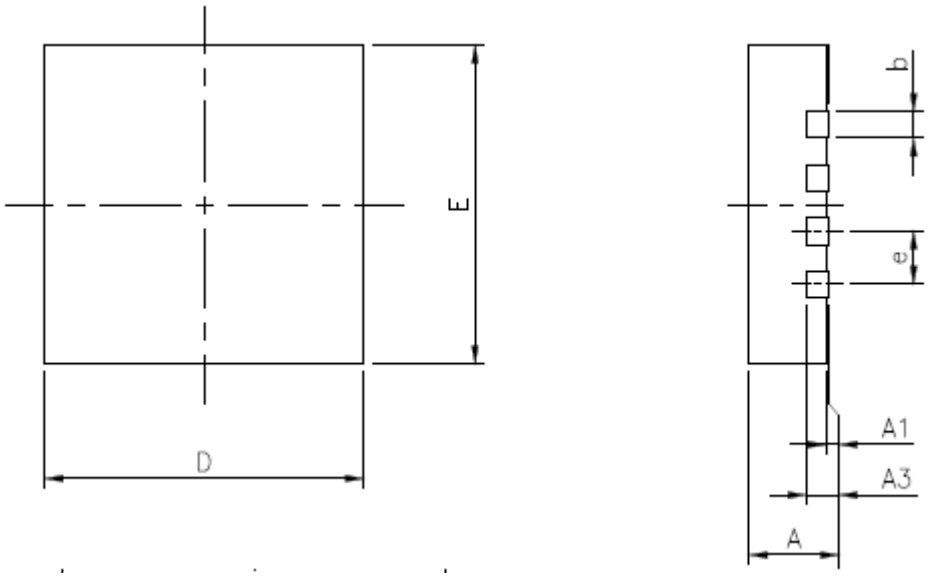
NOTES:
1. JEDEC OUTLINE : MO-137 AB
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3. DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

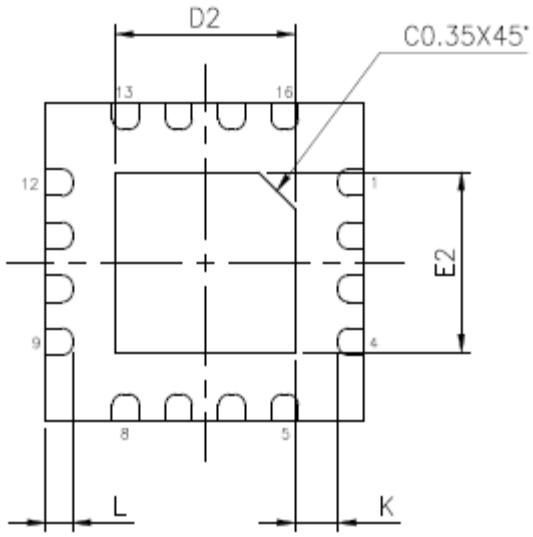
5.2. SOP16 (150mil)



	MILLIMETERS	
SYMBOLS	MIN	MAX
A	-	1.75
A1	0.10	0.25
A2	1.25	-
b	0.31	0.51
c	0.10	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.50
θ °	0	8

5.3. QFN3*3-16





	MILLIMETERS		
SYMBOLS	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.18	0.25	0.30
D		3.00 BSC	
E		3.00 BSC	
e		0.50 BSC	
K	0.20	-	-
D2	1.65	1.70	1.75
E2	1.65	1.70	1.75
L	0.35	0.40	0.45

PKG CODE: WQFN

6. PCB layout guideline

6.1. PCB designer comply with IPC-7525 and IPC-7351 and IPC-7095 requirements is recommended.

6.2. QFN/DFN /SOP E-pad package PCB layout guideline:

6.2.1. Because of the rich solder paste volume under QFN/DFN/SOP thermo pad area which will raise the QFN/DFN package during reflow process, this kind of effect will cause QFN/DFN terminal floating and solderbility fail issue. To prevent the QFN/DFN floating and become solderability open short issue during SMT process, the solder past coverage between 15% to 30 % of thermo pad area is recommended. The blue color areas of Figure QFN/DFN is a just sample for stencil design. Anyway, stencil design should be fine tune by SMT house if the poor contact issue happened.

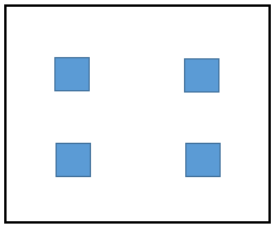


Figure QFN/DFN

6.3. PCB process

6.3.1. Stencil Design Guidelines: Refer to IPC-7525 Stencil Design Guidelines process.

6.3.2. Reflow Oven: Forced convection reflow with nitrogen is recommended for Pb-free and Green package.

6.3.3. Reflow profile: Using more than 8 zone oven is recommended for Pb-free and Green package.

6.3.4. To use IPC-A-610 is recommended for soldered electrical and electronic assemblies.

6.4. Rework and Repair Guide:

6.4.1. Reballing BGA/CSP is not recommended for production applications if there are no special reball fixtures and tools. There are many rework system on market, however, special reball fixtures and tools have been designed to simplify and help control this process. For additional information, refer to IPC -7711/21A Rework and Repair Guide or IPC-7095A (Design & Assembly Process Implementation for BGA's) or search IPC website.

6.4.2. QFN/DFN Rework and Repair Guide: The Rework and Repair Guide of QFN/DFN package is the same with BGA products which need special re-work fixtures and tools, and use IR-reflow process.